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Class	Subclass	ISSUE CLASSIFICATION

PATENT NUMBER

U.S. **UTILITY** Patent Application

O.I.P.E.	PATENT DATE
SCANNED FA TD4 Q.A. TM	

APPLICATION NO.	CONT/PRIOR	CLASS	SUBCLASS	ART UNIT	EXAMINER
09/919372	D	713	798	2182 2133	Chung

APPLICANTS

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TITLE

Clock distribution circuits and methods of operating same that use multiple clock circuits connected by phase detector circuits to generate and synchronize local clock signals

PTO-2040
12/99

ISSUING CLASSIFICATION

ORIGINAL		CROSS REFERENCE(S)	
CLASS	SUBCLASS	CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)

INTERNATIONAL CLASSIFICATION

☐ Continued on Issue Slip Inside File Jacket

☐ TERMINAL DISCLAIMER	DRAWINGS			CLAIMS ALLOWED	
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims	Print Claim for O.G.
☐ The term of this patent subsequent to _____ (date) has been disclaimed.				NOTICE OF ALLOWANCE MAILED	
	(Assistant Examiner)		(Date)		
☐ The term of this patent shall not extend beyond the expiration date of U.S Patent. No. _____				ISSUE FEE	
				Amount Due	Date Paid
	(Primary Examiner)		(Date)		
☐ The terminal ___ months of this patent have been disclaimed.				ISSUE BATCH NUMBER	
	(Legal Instruments Examiner)		(Date)		

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